TSIA 2023半導體獎

獎項介紹

「TSIA 半導體獎」是台灣半導體產業協會於 2014 年起，為了獎勵國內積極從事半導體之學術研究、發明或致力投入產業合作並有具體貢獻者而設立。

此獎項之得獎人由本會遴選委員會評選，遴選委員由在半導體領域已有卓越成就之學者、專家及產業領導者擔任。

今年具博士學位之新進研究人員半導體獎由國立臺灣大學電子工程學研究所吳易忠博士獲獎；博士研究生半導體獎得獎者，分別由臺大、陽明交通、成大、清大、中山等 5 校 11 位博士班同學獲獎，本會期許得獎人以成為台灣半導體產業優秀貢獻者為目標，再接再厲，為台灣半導體產業之永續發展而戮力前進。

贊助單位：理監事公司

力成科技股份有限公司	矽品精密工業股份有限公司
力晶創新投資控股股份有限公司	南亞科技股份有限公司
力晶積成電子製造股份有限公司	凌陽科技股份有限公司
工業技術研究院	創意電子股份有限公司
日月光半導體製造股份有限公司	華邦電子股份有限公司
世界先進積體電路股份有限公司	鈺創科技股份有限公司
立錡科技股份有限公司	漢民科技股份有限公司
台灣積體電路製造股份有限公司	聯發科技股份有限公司
欣銓科技股份有限公司	聯華電子股份有限公司

* 以上依公司筆劃順序排列

吳易忠 Yi-Chung Wu

國立臺灣大學 電子工程學研究所

獲獎摘要

吳易忠博士於 2021 年畢業於國立臺灣大學，其研究領域為數位積體電路與系統設計，主題聚焦於次世代基因定序 (Next-Generation Sequencing) 資料分析硬體加速系統與生醫訊號處理與電路設計。其研究為世界上第一顆適用於次世代基因定序資料分析之系統單晶片，相關研究成果分別發表於 2017, 2020, 2023 IEEE 國際頂尖固態電路會議 ISSCC，並獲選為大會重點論文與榮獲多項國際獎項，包含 2017 ISSCC Silkroad Award, 2019 IEEE SSCS Predoctoral Achievement Award, ISSCC 2020 Takuo Sugano Award for Outstanding Far-East Paper 與 2022 ASSCC Best Student Design Contest Award.

得獎經歷

- 2022 ASSCC Best Student Design Contest Award
- 2022 IEEE 台北分會博士論文獎
- 2022 台灣生醫電子工程協會最佳博士論文優等
- 2021 台灣積體電路設計學會博士論文獎
- 2021 國研院研發服務平台亮點成果獎優等獎
- 2020 ISSCC Takuo Sugano Award for Outstanding Far-East Paper
- 2020 旺宏金矽獎金獎
- 2019 IEEE SSCS Predoctoral Achievement Award
- 2018 TSIA 半導體獎 : 博士研究生
- 2018 聯詠科技博士生獎學金
- 2017 ISSCC Silkroad Award
- 2017 台灣生醫電子工程協會最佳碩士論文優等
- 2016 中國電機工程學會青年論文獎
- 2015 教育部 IE 競賽核心技術組特優
- 2015 教育部 IC 競賽標準元件數位電路設計組特優

重要學術著作

1. Y.-L. Chen, C.-H. Yang, **Y.-C. Wu** (Co-First Author) et al., "A Fully Integrated End-to-End Genome Analysis Accelerator for Next-Generation Sequencing," Int. Solid-State Circuits Conference (ISSCC), pp. 44-45, Feb. 2023.
2. C.-H. Yang, **Y.-C. Wu** et al., "A 75.6M Base-pairs/s FPGA Accelerator for FM-index Based Paired-end Short-Read Mapping," IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2022.
3. Y.-C. Lo, **Y.-C. Wu**, C.-H. Yang, "A 44.3mW 62.4fps Hyperspectral Image Processor for MAV Remote Sensing," Int. Symposium on VLSI Circuits (VLSI Circuits), pp. 74-75, June 2022.
4. **Y.-C. Wu** et al., "A 975mW Fully Integrated Genetic Variant Discovery System-on-Chip in 28nm for Next-Generation Sequencing," IEEE J. Solid-State Circuits (JSSC) ISSCC 2020 Special Issue, vol. 56, no. 1, pp. 123-135, Jan. 2021.
5. **Y.-C. Wu** et al., "A Fully Integrated Genetic Variant Discovery SoC for Next-Generation Sequencing," Int. Solid-State Circuits Conference (ISSCC), pp. 322-323, Feb. 2020.
6. C.-H. Lu, **Y.-C. Wu**, and C.-H. Yang, "A 2.25 TOPS/W Fully-Integrated Deep CNN Learning Processor with On-Chip Training," IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 65-58, Nov. 2019.
7. X.-H. Qian, **Y.-C. Wu** et al., "A Bone-Guided Cochlear Implant CMOS Microsystem Preserving Acoustic Hearing," Proc. Int. Symposium on VLSI Circuits (VLSI Circuits), pp. 46-47, June 2017.
8. **Y.-C. Wu**, J.-H. Hung, C.-H. Yang, "A 135mW Fully Integrated Data Processor for Next-Generation Sequencing," IEEE Trans. Biomedical Circuits and Systems (TBioCAS) ISSCC 2017 Special Issue, vol. 11, no. 6, pp. 1216-1225, Dec. 2017.
9. **Y.-C. Wu**, J.-H. Hung, C.-H. Yang, "A 135mW Fully Integrated Data Processor for Next-Generation Sequencing," Int. Solid-State Circuits Conference (ISSCC), pp. 252-253, Feb. 2017.

指導教授　楊家驤 教授

現職
- Professor, Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University

學歷
- Ph.D. (2010) in Electrical Engineering, University of California at Los Angeles
- M.S. (2004) and B.S. (2002) in Electrical Engineering, National Taiwan University

經歷
- TPC Member, International Solid-State Circuits Conference (ISSCC)
- TPC Member, Symposium on VLSI Circuits (VLSI Circuits)
- TPC Member, Asian Solid-State Circuit Conference (A-SSCC)
- Senior Associate Editor, IEEE Signal Processing Letters (SPL)
- Guest Editor, IEEE Journal of Solid-State Circuits (JSSC)

林鑫成 Hsin-Cheng Lin

國立臺灣大學 電子工程學研究所

獲獎摘要

林鑫成同學於國立臺灣大學電子工程學研究所攻讀博士班，研究領域為先進三維電晶體之數位與射頻特性分析優化，後段製程電路佈局之設計優化，與先進靜態儲存記憶體單元之設計開發。對於三維電晶體如鰭式電晶體 (FinFET)，垂直堆疊閘極環繞式電晶體 (stacked GAAFETs)，與樹狀通道電晶體 (TreeFET) 之數位與射頻特性都有進行設計優化。相關研究成果發表於一流之 IEEE EDL 與 TED 國際期刊，有 13 項美國專利申請中。成果豐碩，難能可貴。

得獎經歷 / 專利

- 2021 台積電博士班獎學金
- 以第一發明人申請 9 篇美國專利，以第二發明人申請 4 篇美國專利
- 2020~2022 台積電 - 臺大聯合研發中心獎助學金
- 2020~2022 鑫淼重點科技博士生獎學金
- 2022 未來科技獎 (FutureTech Award)
- 2021 Dialog 戴樂格半導體獎勵學生優良研究成果獎

重要學術著作

1. **Hsin-Cheng Lin**, Tao Chou, Kung-Ying Chiu, Sun-Rong Jan, Chia-Che Chung, Chia-Jung Tsen, and C. W. Liu, "RF Performance of Stacked Si Nanosheets/Nanowires," IEEE Electron Device Letters, Vol. 43, No. 7, pp. 1017-1020, July 2022.
2. **Hsin-Cheng Lin**, Tao Chou, Chia-Che Chung, Chia-Jung Tsen, Bo-Wei Huang, and C. W. Liu, "RF Performance of Stacked Si Nanosheet nFETs," IEEE Transactions on Electron Devices, Vol. 68, No. 10, pp. 5277-5283, Oct. 2021.
3. **Hsin-Cheng Lin**, Kuan-Ying Chiu, Ching-Wang Yao, Tao Chou, Tsai-Yu Chung, and C. W. Liu, "BEOL Design and RF Performance of Stacked Si Nanosheets and Nanowires," 2023 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2023.
4. **Hsin-Cheng Lin**, Tao Chou, Kung-Ying Chiu, Chia-Che Chung, Chia-Jung Tsen, and C. W. Liu, "RF Performance Optimization of Stacked Si Nanosheet nFETs," 2022 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2022.
5. Chia-Che Chung, **Hsin-Cheng Lin**, H. H. Lin, W. K. Wan, M.-T. Yang, and C. W. Liu, "Interpretable Neural Network to Model and to Reduce Self-Heating of FinFET Circuitry," 2020 Symposium on VLSI Technology (VLSI), 2020.
6. Chia-Che Chung, **Hsin-Cheng Lin**, Bo-Wei Huang, Chia-Jung Tsen, and C. W. Liu, "Architecture and Optimization of 2T (Footprint) SRAM," IEEE Transactions on Electron Devices, Vol. 68, No. 10, pp. 4918-4924, Oct. 2021.
7. Chia-Che Chung, Bo-Wei Huang, **Hsin-Cheng Lin**, Tao Chou, Chia-Jung Tsen, and C. W. Liu, "Self-Heating of FinFET Circuitry Simulated by Multi-Correlated Recurrent Neural Networks," IEEE Electron Device Letters, vol. 43, no. 8, pp. 1179-1182, Aug. 2022.
8. Tao Chou, Chia-Che Chung, **Hsin-Cheng Lin**, and C. W. Liu, "Cell Stability and Write Improvement of 2T (Footprint) Stacked SRAM," 2022 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2022.
9. Chung-En Tsai, Chun-Yi Cheng, Bo-Wei Huang, **Hsin-Cheng Lin**, Tao Chou, Chien-Te Tu, Yi-Chun Liu, Sun-Rong Jan, Yu-Rui Chen, Wan-Hsuan Hsieh, Kung-Ying Chiu, Shee-Jier Chueh, and C. W. Liu, "Nearly Ideal Subthreshold Swing and Delay Reduction of Stacked Nanosheets Using Ultrathin Bodies," Symposium on VLSI Technology and Circuits (VLSI), JUNE 13-17, 2022.
10. Yi-Chun Liu, Yu-Rui Chen, Yun-Wen Chen, **Hsin-Cheng Lin**, Wan-Hsuan Hsieh, Chien-Te Tu, Bo-Wei Huang, Wei-Jen Chen, Chun-Yi Cheng, Shee-Jier Chueh, and C. W. Liu, "Extremely High- κ $Hf_{0.2}Zr_{0.8}O_2$ Gate Stacks Integrated into $Ge_{0.95}Si_{0.05}$ Nanowire and Nanosheet nFETs Featuring Respective Record I_{ON} per Footprint of 9200 μA/μm and Record I_{ON} per Stack of 360 μA at V_{OV}=V_{DS}=0.5V," accepted by Symposium on VLSI Technology and Circuits (VLSI), JUNE 11-16, 2023.

指導教授　劉致為 教授

現職
- Distinguished (特聘) / Chair (講座) Professor, National Taiwan University

學歷
- Ph.D. 1994 Electrical Engineering, Princeton University
- M.S. 1987 and B.S. 1985, National Taiwan University

經歷
- IEEE Fellow (2018~)
- Deputy General Director (副主任 , 2008~2013) / Senior full researcher (資深研究員 , 2011~), National Nano Device Labs
- Research Director / Senior full researcher (資深研究員), ERSO / ITRI (2002~2005)

莊育權 Yu-Chuan Chuang

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獲獎摘要

莊育權同學自 2019 年起碩士逕讀國立臺灣大學電子工程學研究所博士班，研究領域為記憶體內運算 (Computing-in Memory, CIM) 之低功耗 / 抗噪演算法開發以及適用於智慧終端裝置之輕量型 AI 演算法與晶片設計。相關研究成果發表於 IEEE 頂尖國際會議 DAC 和頂尖國際期刊 IEEE JETCAS、TCAS-I、TC。在學期間成果豐碩並獲多項獎項肯定，難能可貴。

得獎經歷

- 2023 第二十三屆旺宏金矽獎 優勝獎
- 2023 台灣半導體研究中心晶片設計 優等設計獎
- 2022 IEEE AICAS Best Student Paper Award
- 2022 國科會補助博士生赴國外研究
- 2022 中技社獎學金
- 2021 南亞科技未來之星獎學金
- 2020 Garmin 獎學金
- 2020 台灣半導體研究中心晶片設計 特優設計獎
- 2019 第十九屆旺宏金矽獎 優勝獎
- 2019 教育部 IC 競賽標準元件數位電路設計組研究所組 特優
- 2018 教育部 IC 競賽標準元件數位電路設計組大學組 特優
- 2018 國科會優秀博士獎學金
- 2018 IEEE IECBES Best Paper Award

重要學術著作

1. Y.-T. Chen, **Y.-C. Chuang**, et al, "S-QRD-ELM: Scalable QR-Decomposition-Based Extreme Learning Machine Engine Supporting Online Class-Incremental Learning for ECG-Based User Identification," in IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I), Mar., 2023.
2. C.-Y. Chang, **Y.-C. Chuang**, et al, "Recent Progress and Development of Hyperdimensional Computing (HDC) for Edge Intelligence," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), Feb., 2023.
3. C.-Y. Chang, K.-C. Chou, **Y.-C. Chuang**, et al, "E-UPQ: Energy-aware Unified Pruning-Quantization Framework for CIM Architecture," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), Feb., 2023.
4. M. G. Lin, C. T. Huang, **Y.-C. Chuang**, et al, "D-NAT: Data-Driven Non-Ideality Aware Training Framework for Fabricated Computing-In-Memory Macros," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), Apr., 2022.
5. C.-Y. Chang[†], **Y.-C. Chuang**[†], et al, "MulTa-HDC: A Multi-Task Learning Framework for Hyperdimensional Computing," in IEEE Transactions on Computers (TC), Apr. 2021.
6. **Y.-C. Chuang**, et al, "An Arbitrarily Reconfigurable Extreme Learning Machine Inference Engine for Robust ECG Anomaly Detection," in IEEE Open Journal of Circuits and Systems, Jan. 2021.
7. C. T. Huang, C.-Y. Chang, **Y.-C. Chuang**, et al, "BWA-NIMC: Budget-based Workload Allocation for Hybrid Near/In-Memory-Computing," in ACM/IEEE Design Automation Conference (DAC), 2023.
8. C.-Y. Chang, **Y.-C. Chuang**, et al, "T-EAP: Trainable Energy-Aware Pruning for NVM-based Computing-in-Memory Architecture," in IEEE International Conference on Artificial Intelligence Circuits & Systems (AICAS), Sep., 2022.
9. **Y.-C. Chuang**, et al, "Dynamic Hyperdimensional Computing for Improving Accuracy-Energy Efficiency Trade-offs," in IEEE International Workshop on Signal Processing Systems (SiPS), Oct. 2020.
10. K. Tung, P.-K. Liu, **Y.-C. Chuang**, et al, "Entropy-Assisted Multi-Modal Emotion Recognition Framework Based on Physiological Signals," in. IEEE-EMBS Conference on Biomedical Engineering and Sciences (IECBES), Dec. 2018.

指導教授　吳安宇 教授

現職
- 國立臺灣大學電機系 / 電子所特聘教授

學歷
- Ph.D. in Electrical Engineering, University of Maryland, 1995
- M.S. in Electrical Engineering, University of Maryland, 1992
- B.S. in Electrical Engineering, National Taiwan University, 1987

經歷
- (IEEE 期刊總主編) Editor-in-Chief (EiC), IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) (2020~2021)
- 國立臺灣大學電子所所長 (2016~2019)
- IEEE Fellow (2015~)
- 工研院系統晶片中心副主任 (2007~2009)
- Member of Technical Staff, AT&T Bell Labs. / Microelectronics (1995~1996)

鄭浩天 Hao-Tien Cheng

國立臺灣大學 電子工程學研究所

獲獎摘要

鄭浩天同學於國立臺灣大學電子工程學研究所攻讀博士班，研究領域為高速半導體雷射與光通訊晶片之元件開發與特性分析。其中包括垂直共振腔面射型雷射 (VCSEL) 以及發光電晶體 (light-emitting transistor) 之製程與優化。相關研究成果發表於 IEEE 及 Optica 頂尖期刊 IEEE JLT、EDL、TED、Optics Express、Optics Letters 等國際期刊。成果豐碩，難能可貴。

得獎經歷 / 專利

- 2023 國立臺灣大學研究所優秀僑生獎學金
- 2022 國科會 - 菁英博士生獎學金 - 量子科技
- 2022 台積電 - 臺大聯合研發中心博士生獎助金
- 2020~2022 國立臺灣大學逕行修讀博士學位學生研究提升計畫獎助金
- 美國專利 US11532923B2 – Vertical-cavity surface emitting laser for emitting a single mode laser beam
- 中華民國專利 I749647– 用以產生單一模態的雷射光的垂直共振腔面射形型雷射裝置
- 與指導教授共同創立「徠晶光電股份有限公司」，已經量產初代產品並獲得天使輪募資，目前正在開發第二代雷射產品

重要學術著作

1. **H.-T. Cheng**, Y.-C. Yang, and C.-H. Wu, "Temperature-insensitive 850-nm dual-mode-VCSEL with 25.1-GHz bandwidth at 85°C," Journal of Lightwave Technology, 2023, DOI: 10.1109/JLT.2023.3263040.
2. **H.-T. Cheng**, S.-Y. Min, Y.-C. Yang, H.-Y. Lin, J.-S. Pan, C.-H. Wu, "Single-mode-VCSEL with a ring-shaped self-aligned recessed metal mode filter," IEEE Electron Device Letters, 2023, DOI: 10.1109/LED.2023.3288935.
3. **H.-T. Cheng**, C.-H. Wu, M. Feng, and C.-H. Wu, "40.1-GHz sub-freezing 850-nm VCSEL: Microwave extraction of cavity lifetimes and small-signal equivalent circuit modeling," Opt. Express, vol. 31, no. 7, pp. 11408–11422, 2023, DOI: 10.1364/OE.486480.
4. **H.-T. Cheng**, J. Qiu, C.-Y. Peng, H.-C. Kuo, M. Feng, and C.-H. Wu, "29 GHz single-mode vertical-cavity surface-emitting lasers passivated by atomic layer deposition," Opt. Express, vol. 30, no. 26, pp. 47553–47566, 2022, DOI: 10.1364/OE.474930.
5. **H.-T. Cheng**, J.-S. Pan, W.-H. Lin, Y.-C. Yang, C.-H. Wu, "Zone-addressable 20 x 20 940-nm VCSEL array with 5-bit binary number pattern," Opt. Lett. 48, 2023, DOI:10.1364/OL.494760.
6. **H.-T. Cheng**, Y.-C. Yang, T.-H. Liu, and C.-H. Wu, "Recent advances in 850 nm VCSELs for high-speed interconnects," Photonics, vol. 9, no. 2, p. 107, 2022, DOI: 10.3390/photonics9020107.
7. T.-H. Liu, **H.-T. Cheng**, J.-Y. Wu, and C.-H. Wu, "Achieving ns-level pulsed operation of up to 6.27 W with a 1.55-μm BH-DFB laser for LiDAR applications," Opt. Lett. 48, 3071-3074, 2023, DOI: 10.1364/OL.494220.
8. C.-Y. Peng, **H.-T. Cheng**, et al., "Performance analyses of photonic-crystal surface-emitting laser: Toward high-speed optical communication," Nanoscale Research Letters, vol. 17, no. 1, p. 90, 2022, DOI: 10.1186/s11671-022-03728-x.
9. C.-Y. Peng, **H.-T. Cheng**, H.-C. Kuo, and C.-H. Wu, "Design and optimization of VCSELs for up to 40-Gb/s error-free transmission through impurity-induced disordering," IEEE Transactions on Electron Devices, vol. 67, no. 3, pp. 1041–1046, 2020, DOI: 10.1109/ted.2020.2966364.
10. M.-J. Li, K. Li, X. Chen, S. K. Mishra, A. A Juarez, J. E Hurley, J. S Stone, C.-H. Wang, **H.-T. Cheng** et al., "Single-Mode VCSEL Transmission for Short Reach Communications," Journal of Lightwave Technology, vol. 39, no. 4, pp. 868-880, 2021, DOI: 10.1109/JLT.2020.3028972.

指導教授　吳肇欣 教授

現職　・國立臺灣大學 / 電機系、電子所、光電所、重點科技研究學院
學歷　・美國伊利諾大學香檳分校 / 電機工程博士
經歷　・國立臺灣大學 / 教授
・國立臺灣大學 / 重點科技研究學院 - 元件材料與異質整合學位學程主任
・IEEE 光電學會台北分會 / 副主席
・國立臺灣大學 / 電機資訊學院 - 何宜慈傑出青年學者
・國立臺灣大學 / 電機資訊學院 - 學術貢獻獎
・美國伊利諾大學香檳分校 / 博士後研究員
・美國伊利諾大學香檳分校 / Nick and Katherine Holonyak, Jr. Graduate Research Award

王資文 Tz-Wun Wang

國立陽明交通大學 電機工程學系

獲獎摘要

王資文同學於國立陽明交通大學電機工程學系攻讀博士班。研究領域為第三代半導體氮化鎵元件電路，在氮化鎵驅動器、氮化鎵單片直流降壓升壓轉換器、氮化鎵電路保護機制等等電路已有諸多重大突破研究，目前已獲刊登 2 篇 IEEE Journal of Solid-State Circuits (JSSC) 與 4 篇 IEEE International Solid-State Circuits Conference (ISSCC) 頂級國際論文，其中一篇為 ISSCC 2022 年年度亮點論文 (Highlight Paper)。

得獎經歷

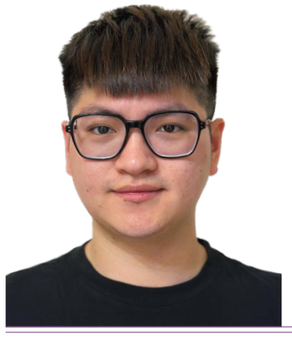
- 2022 ISSCC 大會亮點論文
- 2022 國科會優秀博士生獎學金
- 2022 第二十二屆旺宏金矽獎 - 評審團銀獎
- 2022 交大 - 台積電聯合研發中心獎助金獲獎

重要學術著作

1. **Tz-Wun Wang**, Yu-Yung Kao, Sheng-Hsi Hung, Yong-Hwa Wen, Tzu-Hsien Yang, Si-Yi Li, Ke-Horng Chen, Kuo-Lin Zheng, Ying-Hsi Lin, Shian-Ru Lin and Tsung-Yen Tsai, "Monolithic GaN-Based Driver and GaN Switch With Diode-Emulated GaN Technique for 50-MHz Operation and Sub-0.2-ns Deadtime Control," in IEEE Journal of Solid-State Circuits, vol. 57, no. 12, pp. 3877-3888, Dec. 2022.
2. **Tz-Wun Wang**, Si-Yi Li, Sheng-Hsi Hung, Tzu-Ying Wu, Chi-Yu Chen, Po-Jui Chiu, Ke-Horng Chen, Kuo-Lin Zheng, Ying-Hsi Lin, Tsung-Yen Tsai and Shian-Ru Lin, "Multiple-phase Accelerated Current Control in Bidirectional Energy Transfer of Automotive High-voltage and Low-voltage Batteries," 2023 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 308-310.
3. Yong-Hwa Wen, **Tz-Wun Wang**, Tzu-Hsien Yang, Sheng-Hsi Hung, Kuo-Lin Zheng, Ke-Horng Chen, Ying-Hsi Lin, Shian-Ru Lin and Tsung-Yen Tsai, "A -10 to -20-V Inverting Buck-Boost Drive GaN Driver With Sub-1-μA Leakage Current Vth Tracking Technique for 20-MHz Depletion-Mode GaN Metal–Insulator–Semiconductor High-Electron-Mobility Transistors," in IEEE Journal of Solid-State Circuits, vol. 58, no. 2, pp. 497-507, Feb. 2023.
4. Yu-Yung Kao, **Tz-Wun Wang**, Sheng-Hsi Hung, Yong-Hwa Wen, Tzu-Hsien Yang, Si-Yi Li, Ke-Horng Chen, Ying-Hsi Lin, Shian-Ru Lin and Tsung-Yen Tsai, "A Monolithic GaN-Based Driver and GaN Power HEMT with Diode-Emulated GaN Technique for 50MHz Operation and Sub-0.2ns Deadtime Control," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 228-230.
5. Si-Yi Li, Wei-Chien Hung, **Tz-Wun Wang**, Ya-Ting Hsu, Ke-Horng Chen, Kuo-Lin Zheng, Ying-Hsi Lin, Shian-Ru Lin and Tsung-Yen Tsai, "A High Common-Mode Transient Immunity GaN-on-SOI Gate Driver for High dV/dt SiC Power Switch," 2023 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 302-304.
6. Shu-Yung Lin, Ssu-Yu Lin, Sheng-Hsi Hung, **Tz-Wun Wang**, Ching-Ho Li, Chang-Lin Go, Shao-Chang Huang, Ke-Horng Chen, Kuo-Lin Zheng, Ying-Hsi Lin, Shian-Ru Lin and Tsung-Yen Tsai, "A GaN Gate Driver with On-chip Adaptive On-time Controller and Negative Current Slope Detector," 2023 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 306-308.

指導教授　陳科宏 講座教授

現職　・國立陽明交通大學 / 電機工程學系
學歷　・國立臺灣大學 / 電機工程學系博士
經歷　・國立陽明交通大學電機工程學系教授 / 特聘教授 / 講座教授 (2011/8~ 迄今、2019/5~2022/7、2022/8~ 迄今)
・國立陽明交通大學 / 電機工程學系系主任 (2016/8~2021/7)
・國立陽明交通大學 / 電控工程研究所所長 (2013/8~2016/7)



梁晏旗 Yan-Kui Liang

國立陽明交通大學 國際半導體產業學院

獲獎摘要

梁晏旗同學於國立陽明交通大學國際半導體產業學院攻讀博士班，研究領域為高效能非晶氧化物薄膜電晶體(Amorphous oxide semiconductor Thin-Film Transistors)與鐵電薄膜電晶體(Ferroelectric Thin-Film Transistors)之製程整合與元件特性分析。迄今，相關研究成果發表於IEEE 頂尖國際會議 Symposium on VLSI Technology and Circuits 並以第一作者共發表 5 篇 SCI 國際期刊於 IEEE EDL / IEEE TED 等國際期刊。梁同學於 2022 年獲「國科會補助博士生赴國外研究」，將以訪問學者身分前往日本東京大學進行研究。

得獎經歷

- 2022 國科會補助博士生赴國外研究
- 2022 鴻海科技獎獎學金
- 2022 交大 - 台積電聯合研發中心研究助理獎學金
- 2021 交大 - 台積電聯合研發中心研究助理獎學金
- 2019 國立交通大學卓越博士獎學金

重要學術著作

1. **Y.-K. Liang**, J.-Y. Zheng, Y.-L. Lin, W.-L. Li, Y.-C. Lu, D.-R. Hsieh, L.-C. Peng, T.-T. Chou, C.-C. Kei, C.-C. Lu, H.-Y. Huang, Y.-C. Tseng, T.-S. Chao, E. Y. Chang, C.-H. Lin, "Aggressively Scaled Atomic Layer Deposited Amorphous $InZnO_x$ Thin Film Transistor Exhibiting Prominent Short Channel Characteristics (SS= 69 mV/dec.; DIBL = 27.8 mV/V) and High G_m (802 μS/μm @V_{DS} = 2V) ", 2023 Symposium on Symposium on VLSI Technology and Circuits, 2023.
2. **Y.-K. Liang**, W.-L. Li, J.-W. Lin, Y.-J. Wang, Y.-H. Chu, C.-C. Lu, H.-Y. Huang, Y.-M. Lin, E. Y. Chang, C.-H. Lin, "ZrO_2-HfO_2 Superlattice Ferroelectric Capacitors with Optimized Annealing to Achieve Extremely High Polarization Stability" IEEE Electron Device Letters, vol. 43, no. 9, pp. 1451-1454, Sept. 2022.
3. **Y.-K. Liang**, J.-S. Wu, C.-Y. Teng, H.-L. Ko, Q.-H. Luc, C.-J. Su, E. Y. Chang, C.-H. Lin, "Demonstration of Highly Robust 5 nm $Hf_{0.5}Zr_{0.5}O_2$ Ultra-Thin Ferroelectric Capacitor by Improving Interface Quality," IEEE Electron Device Letters, vol. 42, no. 9, pp. 1299-1302, Sept. 2021.
4. **Y.-K. Liang**, J.-W. Lin, L.-C. Peng, Y. M. Hua, T.-T. Chou, C.-C. Kei, C.-C. Lu, H.-Y. Huang, S. H. Yeong, Y.-M. Lin, P.-T. Liu, E. Y. Chang, C.-H. Lin, "Electrical Characteristics of Ultrathin InZnO Thin-Film Transistors Prepared by Atomic Layer Deposition," IEEE Transactions on Electron Devices, vol. 70, no. 3, pp. 1067-1072, March 2023.
5. **Y.-K. Liang**, Y.-S. Huang, L.-C. Peng, T.-Y. Yang, B.-F. Young, C.-C. Lu, S. H. Yeong, Y.-M. Lin, C.-J. Su, E. Y. Chang, C.-H. Lin, "Effects of Annealing Temperature on TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN Ferroelectric Capacitors Prepared by In-situ like Consecutive Atomic Layer Deposition," IEEE Transactions on Nanotechnology, vol. 21, pp. 328-331, 2022.
6. **Y.-K. Liang**, J.-W. Lin, Y.-S. Huang, W.-C. Lin, B.-F. Young, Y.-C. Shih, C.-C. Lu, S. H. Yeong, Y.-M. Lin, P.-T. Liu, E. Y. Chang, C.-H. Lin, "Characterization of Ferroelectric characteristics for Hafnium Zirconium Oxide Capacitors with Refractory Electrodes," ECS Journal of Solid State Science and Technology, vol. 11, no. 5, pp. 053012, Mar. 2022.
7. M.-L. Kao, **Y.-K. Liang**, et. al, "IGZO Thin-Film Transistor with HfO_2/Al_2O_3/AlN Hybrid Gate Dielectric Stack Exhibiting Ferroelectric-Like Behavior" IEEE Electron Device Letters, vol. 43, no. 12, pp. 2105-2108, Dec. 2022.
8. T.-Y. Yang, H.-Y. Huang, **Y.-K. Liang**, et. al, "A Normally-Off GaN MIS-HEMT Fabricated Using Atomic Layer Etching to Improve Device Performance Uniformity for High Power Applications," IEEE Electron Device Letters, vol. 43, no. 10, pp. 1629-1632, Oct. 2022.
9. J.-S. Wu, ... **Y.-K. Liang**, et. al, "Superior Breakdown, Retention, and TDDB Lifetime for Ferroelectric Engineered Charge Trap Gate E-mode GaN MIS-HEMT," 2022 International Electron Devices Meeting, San Francisco, CA, USA, 2022.
10. J.-S. Wu, ... **Y.-K. Liang**, et. al, "Hf-based and Zr-based Charge Trapping Layer Engineering for E-Mode GaN MIS-HEMT Using Ferroelectric Charge Trap Gate Stack," IEEE Journal of the Electron Devices Society, vol. 10, pp. 525-531, 2022.

指導教授　林群雄 教授

現職　・國立陽明交通大學 / 國際半導體產業學院
學歷　・Ph.D. Materials Science & Engineering, UIUC, 2000
　　・M.S. Materials Science & Engineering, Rutgers University, 1995
　　・B.S. Materials Science & Engineering, NTHU, 1990
經歷　・Manager, TSMC
　　・Staff Engineer, Northrop Grumman Aerospace System. CA, USA
　　・R&D Engineer, Wireless Semiconductor Division, Agilent Technologies Inc. (i.e., Avago Technologies/now Broadcom, USA)
　　・Sr. Engineer, Portland Technology Development, Intel Corporation, USA

黃欣慧 Hsin-Hui Huang

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獲獎摘要

黃欣慧同學於 2018 年在國立陽明交通大學電子研究所攻讀博士班。研究領域專注在鐵電記憶體之物理模型開發和應用以及可靠度劣化議題之探究。研究成果包含以第一作者發表的 2 篇 IEDM 國際會議論文及 1 篇 IEEE TED 國際期刊論文。和台積電、工研院進行產學合作計畫期間也發表了 4 篇 IEDM 國際會議論文。於 2021 年發表在 VLSI-TSA 的論文還獲得了 Best Student Award。

得獎經歷

- 2022 國立陽明交通大學「第 27 屆科林研發論文獎」博士論文頭等獎
- 2022 國立陽明交通大學「博士論文優等獎」
- 2022 國科會「補助國內研究生參與國際學術會議」獎學金
- 2022 國立陽明交通大學 電機學院研究所「優秀畢業生獎」
- 2021 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) Best Student Paper Award
- 2021 國立陽明交通大學 電機學院「博通獎學金」
- 2019「傑出人才基金會」獎學金

重要學術著作

1. **H.-H. Huang**, et al., "Modeling Fatigue-Breakdown Dilemma in Ferroelectric Hf0.5Zr0.5O2 and Optimized Programming Strategies," in IEEE International Electron Devices Meeting (IEDM), 2022.
2. **H.-H. Huang**, T.-Y. Wu, et al., "A comprehensive modeling framework for ferroelectric tunnel junctions," in 2019 IEEE International Electron Devices Meeting (IEDM), 2019, pp. 32.2. 1-32.2. 4.
3. **H.-H. Huang**, Y.-H. Chu, T.-Y. Wu, M.-H. Wu, I. T. Wang, and T.-H. Hou, "Performance Enhancement and Transient Current Response of Ferroelectric Tunnel Junction: A Theoretical Study," IEEE Transactions on Electron Devices, vol. 69, no. 8, pp. 4686-4692, 2022.
4. Y.-H. Chu, **H.-H. Huang**, et al., "Ultra-thin Hf0.5Zr0.5O2 Ferroelectric Tunnel Junction with High Current Density," in International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2021.
5. T.-Y. Wu, **H.-H. Huang**, et al., "Sub-nA low-current HZO ferroelectric tunnel junction for high-performance and accurate deep learning acceleration," in 2019 IEEE International Electron Devices Meeting (IEDM), 2019: IEEE, pp. 6.3. 1-6.3. 4.
6. M.-H. Yan, M.-H. Wu, **H.-H. Huang**, et al, "BEOL-compatible multiple metal-ferroelectric-metal (m-MFM) FETs designed for low voltage (2.5 V), high density, and excellent reliability," in IEEE International Electron Devices Meeting (IEDM), 2020.
7. C.-C. Chang, **H.-H. Huang**, et al., "Strong Read and Write Interference Induced by Breakdown Failure in Crossbar Arrays," IEEE Transactions on Electron Devices, vol. 67, no. 12, pp. 5497-5504, 2020.
8. C.-C. Chang I.-T. Wang, **H.-H. Huang**, et al., "Strategy of Mitigating Breakdown Interference and Yield Loss in Crossbar Memory," IEEE Transactions on Electron Devices, vol. 68, no. 12, pp. 6082-6086, 2021.
9. Y.-D. Lin, P.-C. Yeh, J.-Y. Dai, J.-W. Su, **H.-H. Huang**, et al., "Highly Reliable, Scalable, and High-Yield HfZrOx FRAM by Barrier Layer Engineering and Post-Metal Annealing," in IEEE International Electron Devices Meeting (IEDM), 2022.
10. J. H. Lee, C. H. Chou, P. J. Liao, Y. K. Chang, **H.-H. Huang**, et al., "Investigation of Defect Engineering Toward Prolonged Endurance for HfZrO Based Ferroelectric Device," in IEEE International Electron Devices Meeting (IEDM), 2022.

指導教授　侯拓宏 講座教授

現職　・國立陽明交通大學 / 電子研究所
學歷　・美國康乃爾大學 / 電機工程博士
經歷　・台灣半導體研究中心 / 主任
　　・IEEE 台北分會理事
　　・科技部 A 世代半導體專案計畫召集人
　　・國立陽明交通大學 / 電子研究所特聘教授
　　・國立陽明交通大學 / 副研發長

洪哲民 Je-Min Hung

國立清華大學 電機工程學系

獲獎摘要

自 2020 年起，洪哲民同學在國立清華大學電機工程學系攻讀博士學位，主攻人工智能晶片的記憶體內運算電路設計。研究範疇包含靜態隨機存取記憶體內運算設計、電阻式記憶體內運算設計，以及軟硬體協同運算設計 (software-hardware co-design)，其研究成果曾在 Nature Electronics、JSSC、ISSCC 和 IEDM 等國際知名期刊與會議上發表。同時，洪哲民同學亦參與其他研究專案，如自旋磁性記憶體、鐵電記憶體、相變化記憶體、三維單晶整合運算晶片 (Monolithic 3D-IC) 等。

得獎經歷

- 2021 旺宏金矽獎 – 銅獎
- 2021 台積電 2H 研究助理獎助金獲獎
- 2020 台積電博士生獎學金
- 2020 清華大學校長獎學金

重要學術著作

1. W.-H. Huang, T.-H. Wen, **J.-M. Hung** (Speaker), W.-S. Khwa, et al., "16.6 A Nonvolatile AI-Edge Processor with 4MB SLC-MLC Hybrid-Mode ReRAM Compute-in-Memory Macro and 51.4-251TOPS/W, " 2023 IEEE International Solid- State Circuits Conference (ISSCC), 2023, pp. 258-260.
2. **J.-M. Hung** (Speaker) et al., "An 8-Mb DC-Current-Free Binary-to-8b Precision ReRAM Nonvolatile Computing-in-Memory Macro using Time-Space-Readout with 1286.4-21.6TOPS/W for Edge-AI Devices," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 1-3.
3. C.-X. Xue, **J.-M. Hung** (Speaker), et al., "16.1 A 22nm 4Mb 8b-Precision ReRAM Computing-in-Memory Macro with 11.91 to 195.7TOPS/W for Tiny AI Edge Devices," 2021 IEEE International Solid- State Circuits Conference (ISSCC), 2021, pp. 245-247.
4. T.-C. Chang, ... **J.-M. Hung**, et al., "13.4 A 22nm 1Mb 1024b-Read and Near-Memory-Computing Dual-Mode STT-MRAM Macro with 42.6GB/s Read Bandwidth for Security-Aware Mobile Devices," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 224-226.
5. **Hung, JM.**, Xue, CX., Kao, HY. et al. A four-megabit compute-in-memory macro with eight-bit precision based on CMOS and resistive random-access memory for AI edge devices. Nat Electron 4, 921–930 (2021).
6. **J.-M. Hung** et al., "8-b Precision 8-Mb ReRAM Compute-in-Memory Macro Using Direct-Current-Free Time-Domain Readout Scheme for AI Edge Devices," in IEEE Journal of Solid-State Circuits, vol. 58, no. 1, pp. 303-315, Jan. 2023.
7. **J.-M. Hung**, C.-J. Jhang, P.-C. Wu, Y.-C. Chiu and M.-F. Chang, "Challenges and Trends of Nonvolatile In-Memory-Computation Circuits for AI Edge Devices," in IEEE Open Journal of the Solid-State Circuits Society, vol. 1, pp. 171-183, 2021.
8. **J.-M. Hung**, X. Li, J. Wu and M.-F. Chang, "Challenges and Trends in Developing Nonvolatile Memory-Enabled Computing Chips for Intelligent Edge Devices," in IEEE Transactions on Electron Devices, vol. 67, no. 4, pp. 1444-1453, April 2020.
9. Xue, CX., Chiu, YC., Liu, TW. ... **Hung, JM.**, et al. A CMOS-integrated compute-in-memory macro based on resistive random-access memory for AI edge devices. Nat Electron 4, 81–90 (2021).
10. F.-K. Hsueh, **J.-M. Hung**, et al., "First Demonstration of Ultrafast Laser Annealed Monolithic 3D Gate-All-Around CMOS Logic and FeFET Memory with Near-Memory-Computing Macro," 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2020, pp. 40.4.1-40.4.4.

指導教授　張孟凡 教授

現職
- 國立清華大學 / 電機工程學系特聘教授
- 台灣積體電路製造公司（TSMC）Director of Corporate Research

學歷
- 國立陽明交通大學 / 電子工程博士

經歷
- IEEE Fellow（2019 年）
- 台灣積體電路製造公司（TSMC）Director of Corporate Research（2020~）
- International Solid-State Circuit Conference (ISSCC), Chair of Memory sub-committee (2021~)
- International Electron Devices Meeting (IEDM), Executive Committee (2018~)
- IEEE Taipei Section Chair (2019/1-2021/1)
- 科技部 Program Director, Micro-Electronics Engineering Program (2018/1~2020/12)
- 國立清華大學 / 電機工程學系特聘教授（2019/8~）
- 國立清華大學 / 電機工程學系教授（2014/8）
- 國立清華大學 / 電機工程學系副教授（2006/8）

彭皓楷 Hao-Kai Peng

國立清華大學 工程與系統科學系

獲獎摘要

彭皓楷同學於 2020 年學士提前畢業逕讀國立清華大學工程與系統科學系博士班，其主要研究領域為改善氧化鉿鋯鐵電記憶體介面特性以提升可靠度，並進一步探討鐵電元件在反覆操作過程中遇到多位階儲存能力衰退情形。迄今為止，其研究成果已經以第一作者身分發表於 Applied Physic Letter、IEEE EDL / TED 與 ACS Applied Materials & Interfaces 等知名期刊共 8 篇。

得獎經歷

- 2022 中技社研究獎學金
- 2022 台積電清大研究助理獎助金
- 2021 台積電清大研究助理獎助金
- 2020 台積電博士班獎學金
- 2020 國科會培育優秀博士生獎學金

重要學術著作

1. **H. K. Peng**, C. Y. Chan, K. Y. Chen, and Y. H. Wu, "Enabling Large Memory Window and High Reliability for FeFET Memory by Integrating AlON Interfacial Layer," Appl. Phys. Lett., vol. 118, no. 10, p. 103503, Feb. 2021.
2. **H. K. Peng**, Y. K. Huang, C. P. Chou, and Y. H. Wu, "Recognizing Spatiotemporal Features by a Neuromorphic Network with Highly Reliable Ferroelectric Capacitors on Epitaxial GeSn Film," ACS Appl. Mater. Interfaces, vol. 13, no. 22, pp. 26630-26638, May 2021.
3. **H. K. Peng**, T. H. Kao, Y. C. Kao, P. J. Wu, and Y. H. Wu, "Reduced Asymmetric Memory Window Between Si-Based n- and p-FeFETs With Scaled Ferroelectric $HfZrO_x$ and AlON Interfacial Layer," IEEE Electron Device Lett., vol. 42, no. 6, pp. 835-838, Jun. 2021.
4. **H. K. Peng**, T. C. Lai, T. H. Kao, and Y. H. Wu, "Improved Reliability and Read Latency Under Radiation Observed in $HfZrO_x$ Based p-FeFETs With AlON Interfacial Layer," IEEE Electron Device Lett., vol. 43, no. 3, pp. 494-497, Mar. 2022.
5. **H. K. Peng**, C. Y. Chiu, Y. C. Kao, P. J. Wu, and Y. H. Wu, "Enhanced Reliability, Switching Speed and Uniformity for Ferroelectric $HfZrO_x$ on Epitaxial Ge Film by Post Deposition Annealing for Oxygen Vacancy Control," IEEE Trans. Electron Devices, vol. 69, no. 7, pp. 4002-4009, May 2022.
6. **H. K. Peng**, C. M. Liu, Y. C. Kao, P. J. Wu, and Y. H. Wu, "Improved Immunity to Sub-Cycling Induced Instability for Triple-Level Cell Ferroelectric FET Memory by Depositing $HfZrO_x$ on NH_3 Plasma-Treated Si," IEEE Electron Device Lett., vol. 43, no. 8, pp. 1219-1222, Aug. 2022.
7. **H. K. Peng**, J. Z. Chen, and Y. H. Wu, "Improved Memory Window and Robust Endurance for Ge P-Channel Ferroelectric FET Memory Using Microwave Annealing Followed by Rapid Thermal Annealing," IEEE Electron Device Lett., vol. 43, no. 12, pp. 2073-2076, Dec. 2022.
8. **H. K. Peng**, T. C. Lai, Y. C. Kao, C. M. Liu, P. J. Wu, and Y. H. Wu, "Improved Reliability for Back-End-of-Line Compatible Ferroelectric Capacitor With 3 Bits/Cell Storage Capability by Interface Engineering and Post Deposition Annealing," IEEE Electron Device Lett., vol. 43, no. 12, pp. 2180-2183, Dec. 2022.
9. Y. C. Kao, **H. K. Peng**, Y. K. Wang, K. A. Wu, C. Y. Wang, Y. D. Lin, T. C. Lai, Y. H. Wu, C. Y. Lin, S. W. Hsiao, M. H. Lee, and P. J. Wu, "Toward Highly Pure Ferroelectric $Hf_{1-x}Zr_xO_2$ Thin Films by Tailoring the Strain in an Unstable Thermodynamic System," ACS Appl. Electron. Mater., vol. 4, no. 8, pp. 3897-3908, Aug. 2022.
10. S. C. Yan, C. H. Wu, C. J. Sun, X. C. Zhong, C. S. Chang, **H. K. Peng**, Y. H. Wu, and Y. C. Wu, "Multilevel Cell Ferroelectric HfZrO FinFET with High Speed and Large Memory Window Using AlON Interfacial Layer," IEEE Electron Device Lett., vol. 44, no. 1, pp. 44-47, Jan. 2023.

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- 國立清華大學 / 副教務長
- 國立清華大學 / 工程與系統科學系主任
- 國立清華大學 / 副學務長
- 國立清華大學 / 推廣教育中心主任
- 國立清華大學 / 原子科學院學士班主任
- IET Fellow / IEEE Senior Member

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獲獎摘要

李承穎於博士班就讀期間致力研究壓電與記憶體材料開發、MEMS 元件與製程設計、CMOS 電阻式記憶體與物理密鑰設計、MEMS & CMOS SiP 系統整合等技術。相關研究成果已獲得近 10 件產學合作 (含上市櫃公司)、專利授權、衍生新創公司、大型投資案、國家級獎項、全國性獎項與發明專利數件。並帶領不同領域的實驗室團隊執行諸多國家大型計畫，成功開發出多項世界首創之關鍵技術，相關成果屢獲媒體報導與多次受邀參展，同時亦與知名企業簽署產品大量採購書，準備進行商轉階段。此外，在學術成果上，三年內已發表十餘篇國際指標性重點期刊，對於產業界與學術界均有卓越事蹟。

得獎經歷 / 專利

- 2023 新創科技公司創辦人
- 2022 旺宏金矽獎 : 評審團銅獎
- 2021 科技部未來科技突破獎
- 2020 旺宏金矽獎 : 優勝
- 2019 科技部未來科技突破獎
- 2021~2023 已獲證發明專利：2 件 (中華民國)
- 2022~2023 申請中發明專利：4 件 (中華民國 2 件、美國 1 件、中國 1 件)
- 國家大型計劃 : 半導體射月計畫、深耕計畫、智慧機械計畫

重要學術著作

1. **Cheng-Ying Li**, Ze-Hui Chen, Hsueh-Yu Kao, Sheng-Kai Chang, Po-Yu Hsiao, Yen-Hsiang Huang, Yu-Chieh Huang, Sheng-Yuan Chu, Chia-Ling Wei, Yun-Hui Liu, Kuang-Wei Cheng, Cheng-Che Tsai , "Design and Development of a Low-Power Wireless MEMS Lead-Free Piezoelectric Accelerometer System." IEEE Transactions on Instrumentation and Measurement 72 (2023): 1-11.
2. **Cheng-Ying Li**, Cheng-Che Tsai, Sheng-Yuan Chu, "Mg doping effects on the microstructure and piezoelectric characteristics of ZnO: Li films deposited at room temperature using an RF sputtering deposition method." Ceramics International, 2023, 49.4: 5854-5860.
3. Chang, Ting-Jia, **Cheng-Ying Li**, and Sheng-Yuan Chu. "Ta2O5 doping effects on the property improvement of HfOx-based RRAMs using co-sputtering deposition method." Materials Characterization 199 (2023): 112786.
4. **Cheng-Ying Li**, Yueh-Han Chen, Zhi-Yuan Wei, Yi-Chen Ho, Sheng-Yuan Chu, Cheng-Che Tsai, Cheng-Shong Hong, "Design of a Square MEMS Piezoelectric Accelerometer With a Wide Range of Applicability, a Low Transverse Sensitivity Ratio, and High Accuracy," in IEEE Sensors Journal, vol. 22, no. 10, pp. 9306-9312, 15 May15, 2022, doi: 10.1109/JSEN.2022.3161671.
5. Kao-Peng Min, **Cheng-Ying Li**, Ting-Jia Chang, Sheng-Yuan Chu, "The Effects of Si Doping on the Endurance and Stability Improvement of AlN-Based Resistive Random Access Memory," ACS Applied Electronic Materials, vol. 3, no. 12, pp. 5327-5334, 2021/12/28 2021.
6. Pei-Hao Hung, **Cheng-Ying Li**, Kao-Peng Min, Sheng-Yuan Chu, "Investigations of the Effects of the Orientation of AlN-Based Complementary Resistive Switches," in IEEE Transactions on Electron Devices, vol. 68, no. 8, pp. 3826-3831, Aug. 2021, doi: 10.1109/TED.2021.3086444.
7. Ze-Hui Chen, **Cheng-Ying Li**, Yueh-Han Chen, Sheng-Yuan Chu, Cheng-Che Tsai, Cheng-Shong Hong "Enhancement of c-Axis Oriented Aluminum Nitride Films via Low Temperature DC Sputtering," in IEEE Sensors Journal, vol. 21, no. 16, pp. 17673-17677, 15 Aug.15, 2021, doi: 10.1109/JSEN.2021.3077274.
8. **Cheng-Ying Li**, Chun-Cheng Lin, Sheng-Yuan Chu, Jun-Ting Lin, Chih-Yu Huang, Cheng-Shong Hong "Effects of Nb doping on switching-voltage stability of zinc oxide thin films." Journal of Applied Physics 128.17 (2020): 175308.
9. Ze-Hui Chen, **Cheng-Ying Li**, Sheng-Yuan Chu, Cheng-Che Tsai, Yi-Hsun Wang, Hsueh-Yu Kao, Chia-Ling Wei, Yen-Hsiang Huang, Po-Yu Hsiao, Yun-Hui Liu "The Design of Aluminum Nitride-Based Lead-Free Piezoelectric MEMS Accelerometer System," in IEEE Transactions on Electron Devices, vol. 67, no. 10, pp. 4399-4404, Oct. 2020, doi: 10.1109/TED.2020.3019230.
10. Pei-Hao Hung, **Cheng-Ying Li**, Kao-Peng Min, Chun-Cheng Lin, Sheng-Yuan Chu "Investigations of the effects and mechanisms of metal interconnection layer of AlN-based complementary resistive switches."

指導教授　朱聖緣 教授

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經歷　・國立成功大學 / 電機系特聘教授
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獲獎摘要

張書維同學於國立成功大學電機工程研究所攻讀博士班，在學期間致力於異質通道材料堆疊式互補場效電晶體 (Hybrid Complementary Field-Effect Transistors, Hybrid CFET) 結構開發，並將其應用延伸至快閃記憶體 (Flash Memory)、靜態隨機存取記憶體 (Static Random-Access Memory, SRAM) 及射頻元件 (Radio-Frequency Integrated Circuit, RFIC)，對於系統整合型面板 (System on Panel, SoP) 以及三維一體化電路 (Monolithic Three-Dimensional Integrated Circuit, M3D-IC) 領域貢獻良多，相關研究成果多次發表於頂尖國際會議 Symposium on VLSI Technology、IEDM，以及一流國際期刊 IEEE TED。

得獎經歷 / 專利

- 2021 國研院研發服務平台亮點成果獎特優
- 2020 台積電博士獎學金
- 2019 國研院傑出科技貢獻獎學術研究類佳作
- 2019 科技部 - 培育優秀博士生獎學金
- 2016~2019 台積電 - 成大聯合研發中心獎助學金
- 以第一發明人申請一項美國專利一項中華民國專利

重要學術著作

1. **S.-W. Chang** et al., "First Demonstration of CMOS Inverter and 6T-SRAM Based on GAA CFETs Structure for 3D-IC Applications," 2019 IEEE International Electron Devices Meeting (IEDM), 2019, pp. 11.7.1-11.7.4.
2. **S.-W. Chang** et al., "First Demonstration of Heterogeneous IGZO/Si CFET Monolithic 3D Integration with Dual Workfunction Gate for Ultra Low-power SRAM and RF Applications," 2021 IEEE International Electron Devices Meeting (IEDM), 2021, pp. 34.4.1-34.4.4.
3. X.-R. Yu, M.-H. Chuang, **S.-W. Chang** et al., "Integration Design and Process of 3-D Heterogeneous 6T SRAM with Double Layer Transferred Ge/2Si CFET and IGZO Pass Gates for 42% Reduced Cell Size," 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 20.5.1-20.5.4.
4. C.-Y. Yang, ...**S.-W. Chang** et al., "First Demonstration of Heterogeneous L-shaped Field Effect Transistor (LFET) for Angstrom Technology Nodes," 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 20.2.1-20.2.4.
5. X.-R. Yu, ...**S.-W. Chang** et al., "First Demonstration of Vertical Stacked Hetero-Oriented n-Ge (111)/p-Ge (100) CFET toward Mobility Balance Engineering," 2022 IEEE Symposium on VLSI Technology (VLSI).
6. (Invited) **Shu-Wei Chang** et al., "First Demonstration of Heterogeneous IGZO/Si CFET Monolithic 3D Integration with Dual Workfunction Gate for Ultra Low-power SRAM and RF Applications," in IEEE Transactions on Electron Devices (TED), vol. 69, no. 4, pp. 2101-2107, April 2022.
7. Po-Jung Sung, **Shu-Wei Chang**, Chun-Jung Su, Ta-Chun Cho, Fu-Kuo Hsueh, Wen-Hsi Lee, Yao-Jen Lee, and Tien-Sheng Chao, "Fabrication of Vertically Stacked Nanosheet Junctionless Field-Effect Transistors and Applications for the CMOS and CFET Inverters," in IEEE Transactions on Electron Devices (TED), vol. 67, no. 9, pp. 3504-3509, Sept. 2020.
8. **Shu-Wei Chang**, Yu-Ming Chang, Wen-Hsi Lee, Yao-Jen Lee and Darsen D. Lu, "Nanosheet-Compatible Complementary-FET Logic Non-Volatile Memory Device," in ECS Journal of Solid State Science and Technology, Volume 11, Number 9, September 2022.
9. **Shu-Wei Chang**, Jia-Hon Chou, Wen-Hsi Lee, Yao-Jen Lee and Darsen D. Lu, "TCAD-Based RF Performance Prediction and Process Optimization of 3D Monolithically Stacked Complementary FET," in Solid-State Electronics 201, 2023.
10. Md. Aftab Baig, Cheng-Jui Yeh, **Shu-Wei Chang** et al., "3-D Monolithic Stacking of Complementary-FET on CMOS for Next Generation Compute-In-Memory SRAM," in IEEE Journal of the Electron Devices Society, vol. 11, pp. 107-113, 2023.

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・國巨 - 成大共研中心主任
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・德國飛利浦 Aachen Lab. Scientist

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獲獎摘要

吳珮瑜同學於 2018 年起於國立中山大學材料與光電科學學系攻讀博士班，研究期間專注於半導體元件性能優化與可靠度研究，研究對象涵蓋非揮發式記憶體與第三代半導體元件，其中更致力發展超臨界流體製程技術以改善半導體元件性能，相關成果已以第一作者身分發表於共 6 篇國際期刊如 IEEE EDL 與 TED 等，並以第五發明人發表 1 項美國專利與 1 項台灣專利。此外，研究成果因可應用於開發高價值的電子元件與關鍵材料，榮獲 2021 鴻海科技獎。

得獎經歷 / 專利

- 2022 財團法人李長榮教育基金會 - 優秀學生獎
- 2021 鴻海科技獎
- 2021 華立集團獎學金
- 2019~2023 中山科學研究院 - 優秀學生獎助金
- 以第五發明人發表 1 項美國專利 (US 11417511B1) 與 1 項台灣專利 (I784545)

重要學術著作

1. **P.-Y. Wu**, X.-Y. Tsai, T.-C. Chang*, Y.-H. Yeh, W.-C. Huang, K.-C. Chang, T.-M. Tsai*, and J.-W. Huang. "Analysis of Abnormal Current Rise Mechanism in GaN-MIS HEMT With Al_2O_3/Si_3N_4 Gate Insulator Under Hot Switching" IEEE Trans Electron Devices, vol. 69, no. 8, pp. 4218-4223, Aug. 2022, doi: 10.1109/TED.2022.3184905.
2. **P.-Y. Wu**, H.-X Zheng, T.-C Chang*, W.-J Chen, C.-C Yang, W.-C Chen, M.-C Tai, Y.-F Tan, H.-C Huang, X.-H Ma, Y. Hao, T.-M Tsai and S. M. Sze, "Improvement of Resistive Switching Characteristics in Zinc Oxide-Based Resistive Random Access Memory by Ammoniation Annealing," IEEE Electron Device Lett. vol. 41, no. 3, pp. 357-360, Mar. 2020, doi: 10.1109/LED.2020.2968629
3. **P.-Y. Wu**, T.-C Chang*, M.-C. Chen, H.-X Zheng, Y.-S Lin, X.-Y Tsai, K.-J Chang, W.-C Kuo, C.-W Lin and T.-M Tsai*, "Performance and reliability optimization of supercritical-nitridation-treated AlGaN/GaN high-electron-mobility transistors". IEEE Trans Electron Devices, vol. 68, no. 9, pp. 4317-4321, Aug. 2021, doi: 10.1109/TED.2021.3099450
4. S.-Y. Chou, **P.-Y. Wu**, M.-C. Chen, T.-C Chang*, X.-Y. Tsai, S.-K Lin, H.-Yi, Tu, C.-W. Wu, T.-M. Tsai and J. W. Huang, "Performance Improvement by Enhancing Passivation Layer of p-Type GaN High-Electron Mobility Transistors with Supercritical Oxygen Treatment". IEEE Electron Device Letters. vol. 44, no. 2, pp. 213-216, Dec. 2022, doi: 10.1109/LED.2022.3232610 (S.-Y. Chou, P.-Y. Wu contribute equally)
5. **P.-Y. Wu**, T.-C Chang*, M.-C Chen, C. C Yang, H.-X Zheng, P.-H Chen, W.-C Chen, Y.-C Zhang, S.-K Lin, J.-J Chen, H.-C Huang, T.-M Tsai* and S. M Sze "Improvement of Hafnium Oxide Resistive Memory Performance Through Low-Temperature Supercritical Oxidation Treatments". IEEE Trans Electron Devices, vol. 68, no. 2, pp. 541-544, Feb. 2021, doi: 10.1109/TED.2020.3043209
6. **P.-Y. Wu**, M.-C. Chen, T.-C Chang*, H.-X Zheng, F.-Y Jin, Y.-F Tan, Y.-F Tu, X.-Y Tsai, J.-W Huang, K.-J Chang*, G.-S Liu and T.-M Tsai, "Enhancing gate turn-off thyristor blocking characteristics by low temperature defect passivation technology". Semicond Sci Technol, vol. 36, no. 8. pp. 085005, Jun. 2021, doi: 10.1088/1361-6641/ac0b9b
7. **P.-Y. Wu**, X.-Y. Tsai, T.-C. Chang, T.-M. Tsai, and S.-M. Sze, "Comparative study on characteristics of GaN-based MIS-HEMTs with Al_2O_3 and Si_3N_4 gate insulators under Hot Carrier Degradation". 2023 35th International Conference on Microelectronic Test Structure (ICMTS), Apr. 2023, doi: 10.1109/ICMTS55420.2023.10094072
8. Y.-B. Wang, T.-C. Chang*, S.-K. Lin, **P.-Y. Wu**, Y.-C. Zhang, Y.-F. Tan, W.-C. Chen, C.-W. Wu, S.-Y. Chou, K.-J. Zhou, L.-C. Sun, X.-Y. Tsai and Simon M. Sze, "Forming-Free HfO_2-Based Resistive Random Access Memory by X-ray Irradiation, IEEE Trans Electron Devices, vol. 69, no. 12. pp. 6705-6709, Nov. 2022, doi: 10.1109/TED.2022.3215932.
9. S.-K Lin, M.-C. Chen, T.-C. Chang*, C.-H. Lien, C.-H. Wu, Y.-S. Lin, **P.-Y. Wu**, Y.-F. Tan, W.-C. Huang, Y.-C.Zhang, S.-Y Chou, C.-W. Wu and Simon M. Sze, "Use of a supercritical fluid treatment to improve switching region in resistive random access memory." Appl. Phys. Express, vol. 15, no. 6, pp. 064006, Jun. 2022, doi: 10.35848/1882-0786/ac7031.
10. J.-J. Chen, T.-C. Chang*, Y.-H. Hung, Y.-Z. Zheng, C.-W. Kuo, S.-K. Lin, **P.-Y. Wu**, C.-H. Tsai, and Simon Ogier. "Gate Dielectric Leakage Reduction in Hard-Mask Defined and Dry-Etch Patterned Organic TFTs Devices." IEEE Electron Device Lett, vol. 43, no. 1, pp. 48-51, Jan. 2022, doi: 10.1109/LED.2021.3127044.

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經歷　・國立中山大學 / 材料與光電科學學系副教授 (2013~ 迄今)

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現職　・國立中山大學 / 物理系
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